IN THE CLAIMS

1. (Previously presented) A method comprising:

calculating an achieved data transition density for at least one data lane in a point-to-point memory channel having a plurality of data lanes, the achieved data transition density calculated over greater than two clock cycles; and

transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density.

2. (Previously presented) The method of claim 1, wherein calculating an achieved data transition density for the at least one data lane comprises:

counting how many times a data transition occurs on the at least one data lane during a predetermined number of clock cycles, the predetermined number of clock cycles being greater than two.

3. (Original) The method of claim 2, further comprising:

storing a desired data transition density for the at least one data lane; and

comparing the achieved data transition density to the desired data transition density.

4. (Original) The method of claim 3, wherein transmitting a synchronization signal on the at least one data lane responsive to the achieved transition density comprises:

transmitting a synchronization signal on all the data lanes if the achieved data transition density is less then the desired data transition density on the at least one data lane.

5. (Currently Amended) A memory channel comprising:

a host and a plurality of DIMMs connected in a point-to-point fashion, wherein the host includes a processor;

an outbound data channel and an inbound data channel, each having a plurality of data lanes;

at least one transition detection circuit configured to detect whether an achieved data transition density on at least one data lane is less than a desired data transition density for the at least one data lane; and

a transition generator configured to transmit a synchronization signal on the at least one data lane if the achieved transition density is less than the desired data transition density;

wherein the achieved transition density is measured over greater than two clock cycles.

6. (Original) The memory channel of claim 5, wherein the at least one transition detection circuit is located on the host.

7. (Original) The memory channel of claim 5, wherein the at least one transition detection circuit is located on a corresponding one of the plurality of DIMMs.

8. (Original) The memory channel of claim 5, wherein the at least one transition detection circuit comprises:

a plurality of data transition detectors, each configured to detect a data transition on a corresponding data lane;

a clock cycle counter;

a plurality of data transition counters, each configured to count the data transitions detected by a corresponding data transition detector, and configured to be reset by the clock cycle counter;

a logic block configured to signal when at least one of the plurality of data transition counters counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than the desired data transition density.

9. (Original) The memory channel of claim 8, wherein the clock cycle counter and the plurality of data transition counters are programmable.

10. (Original) The memory channel of claim 8, wherein the logic block comprises an AND gate and a plurality of NAND gates.

11. (Original) The memory channel of claim 5, wherein the at least one transition detection circuit comprises:

a plurality of data transition detectors, each configured to detect a data transition on a corresponding data lane;

a clock cycle counter;

a plurality of data transition counters, each configured to count the data transitions detected by a corresponding data transition detector, and configured to be reset by the clock cycle counter;

a first logic block configured to signal when at least one of the plurality of data transition counters corresponding to the data lanes on the outbound data path counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than the desired data transition density; and

a second logic block configured to signal when at least one of the plurality of data transition counters corresponding to the data lanes on the inbound data path counts, during a time period defined by the clock cycle counter, a number of data transitions detected by the corresponding data transition detector that is less than the desired data transition density.

12. (Original) The memory channel of claim 11, wherein the clock cycle counter and the plurality of data transition counters are programmable.

13. (Original) The memory channel of claim 11, wherein the first logic block and the second logic block comprise a plurality of NAND gates and an AND gate.

14. (Currently Amended) An article of machine-readable code, embodied on a machine-readable medium, that when executed causes a machine to perform processes comprising:

storing a desired data transition number;

storing a clock cycle number that is greater than two;

for a data lane in a point-to-point memory channel, recording a measured data transition number over a period of clock cycles equal to the clock cycle number; ~~and~~

comparing the measured data transition number to the desired data transition number; and

transmitting a synchronization signal on the data lane if the measured data transition number is less than the desired data transition number.

15. (Previously presented) The article of machine-readable code of claim 14, that when executed, causes the machine to perform processes further comprising:

transmitting a synchronization signal on the data lane if the measured data transition number is less than the desired data transition number.

16. (Withdrawn) A method comprising:

operating a selected data lane from a point-to-point memory channel having a plurality of data lanes in an inverted mode according to a preselected data inversion scheme.

17. (Withdrawn) The method of claim 16, wherein operating the selected data lane in the inverted mode comprises:

applying data inversions simultaneously to both a receiver and a transmitter of the selected data lane in a node of the point-to-point memory channel.

18. - 21. (Cancelled)

22. (Withdrawn) A machine-readable medium, that when read, causes a machine to perform processes comprising:

operating a selected data lane of a point-to-point memory channel in an inverted mode according to a preselected data inversion scheme.

23. (Withdrawn) The machine-readable medium of claim 22, wherein operating the selected data lane of the point-to-point memory channel in an inverted mode according to a preselected data inversion scheme comprises:

applying data inversions simultaneously to a plurality of receivers and a plurality of transmitters that correspond to the selected data lane, wherein the data inversions are applied according to the preselected data inversion scheme.

24. (Withdrawn) The machine-readable medium of claim 22, that when read, causes the machine to perform processes further comprising:

loading a bit sequence that represents the preselected data inversion scheme into a wraparound shift register.

25. (Currently Amended) The method of claim 1, wherein transmitting the synchronization signal on the at least one data lane comprises:

transmitting the synchronization signal having a number of transitions to cause the achieved data transition density for the at least one data lane to be ~~is~~ greater than or equal to a desired data transition density.

26. (Previously presented) The memory channel of claim 5, wherein for each of the at least one transition detection circuit:

the transition detection circuit is configured to detect whether an achieved data transition density on a corresponding one of the at least one data lane is less than the desired data transition density for the corresponding data lane.

27.-28. (Canceled)